

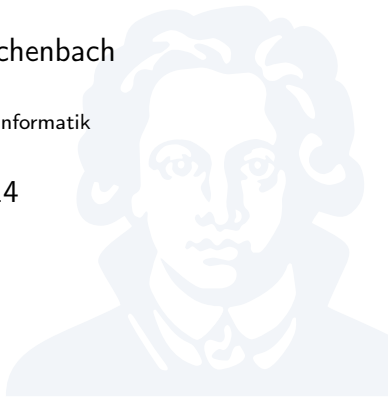
Foundations of Programming Languages

20PM Assembly (1/3): Introduction

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2OPM: Two-Operand Pseudo-MIPS

- ▶ Synthetic Assembly Language
- ▶ Based on MIPS64, but most instructions use only two operands:

```
add $t0, $t1 # $t0 := t0 + t1$ 
```



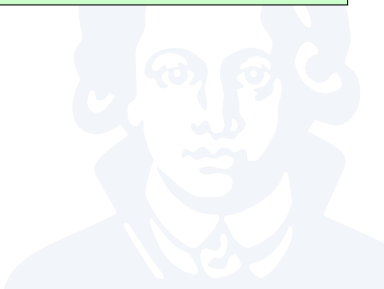
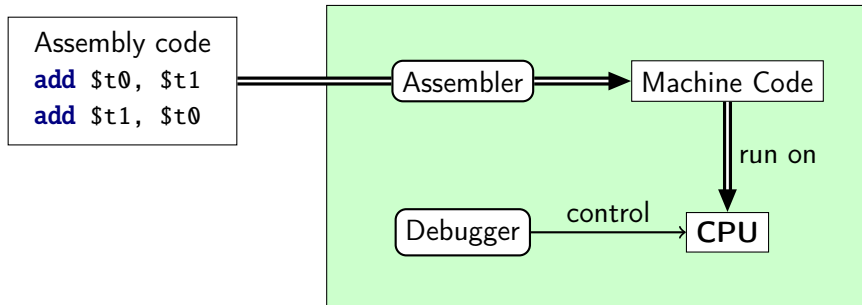
2OPM: Two-Operand Pseudo-MIPS

- ▶ Synthetic Assembly Language
- ▶ Based on MIPS64, but most instructions use only two operands:
`add $t0, $t1 # $t0 := $t0 + $t1`
- ▶ 16 Registers
- ▶ Translates (mostly) directly to Intel 64-bit machine code
⇒ Suitable CPU can execute instructions directly

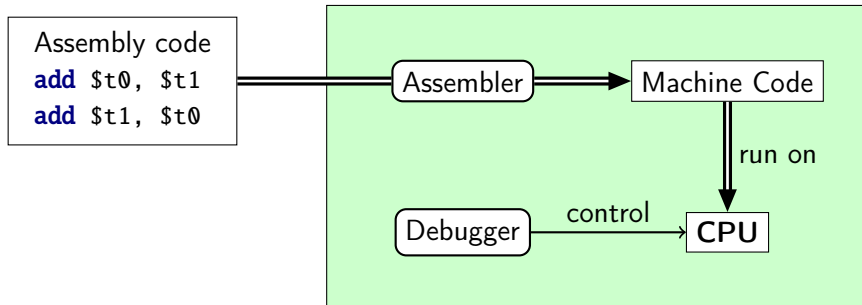
Easier than Intel assembly, almost as efficient



Using 2OPM



Using 2OPM

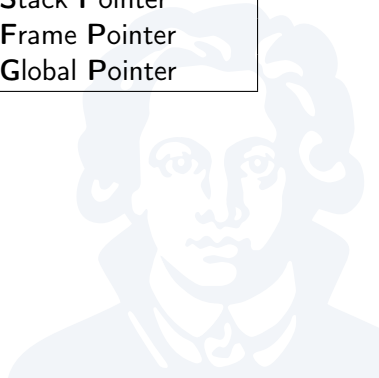


We will also use 2OPM in a language implementation

2OPM Registers

2OPM features 16 general-purpose registers:

Name	Purpose
\$v0	Return Value
\$a0, \$a1, \$a2, \$a3, \$a4, \$a5	Arguments
\$s0, \$s1, \$s2, \$s3	Saved registers
\$t0, \$t1	Temporary registers
\$sp	Stack Pointer
\$fp	Frame Pointer
\$gp	Global Pointer



20PM Registers

20PM features 16 general-purpose registers:

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\$v0	Return Value
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\$fp	Frame Pointer
\$gp	Global Pointer

Plus \$pc:

- ▶ *Program Counter*, address of next instruction
- ▶ can't be referenced directly

Purpose defined by *convention*

Intel 64-bit Registers

64-bit x86 features 16 general-purpose registers:

Name	Purpose
%rax	Return Value
%rdi, %rsi, %rdx, %rcx, %r8, %r9	Arguments
%rbx, %r12, %r13, %r14	Saved registers
%r10, %r11	Temporary registers
%rsp	Stack Pointer
%rbp	Frame Pointer
%r15	Global Pointer

Plus %rip:

- ▶ *instruction pointer*, address of next instruction
- ▶ can't be referenced directly

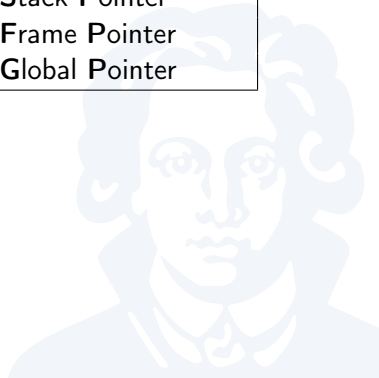
Historical naming; we will use the 2OPM names

2OPM Registers

2OPM features 16 general-purpose registers:

Name	Purpose
\$v0	Return Value
\$a0, \$a1, \$a2, \$a3, \$a4, \$a5	Arguments
\$s0, \$s1, \$s2, \$s3	Saved registers
\$t0, \$t1	Temporary registers
\$sp	Stack Pointer
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\$gp	Global Pointer

Plus \$pc



Basic Operations

```
li    $t0, 2    # $t0 := 2
```

- ▶ **li** \$r, v
Load 64 bit value v into \$r



Basic Operations

```
li    $t0, 2    # $t0 := 2
move  $t1, $t0  # $t1 := $t0
```

- ▶ **li** \$r, v
Load 64 bit value v into \$r
- ▶ **move** \$r0, \$r1
Copy contents of \$r1 into \$r0



Basic Operations

```
li    $t0, 2    # $t0 := 2
move  $t1, $t0  # $t1 := $t0
add   $t0, $t1  # $t0 := $t0 + $t1
```

- ▶ **li** \$r, v
Load 64 bit value v into \$r
- ▶ **move** \$r0, \$r1
Copy contents of \$r1 into \$r0
- ▶ **add** \$r0, \$r1
Add contents of \$r1 into \$r0

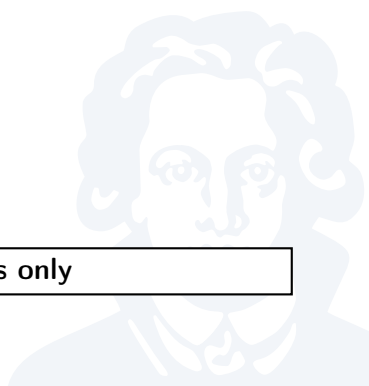


Basic Operations

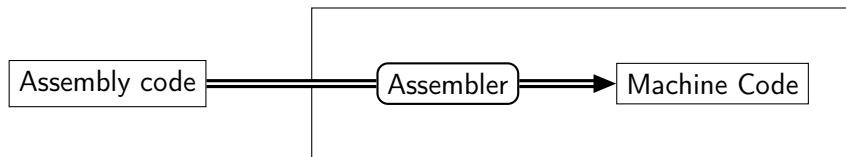
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move  $t1, $t0  # $t1 := $t0
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- ▶ **li** \$r, v
Load 64 bit value v into \$r
- ▶ **move** \$r0, \$r1
Copy contents of \$r1 into \$r0
- ▶ **add** \$r0, \$r1
Add contents of \$r1 into \$r0

Operate on registers only



Machine Code



li	\$t0, 2	49 ba 02 00 00 00 00 00 00 00
move	\$t1, \$t0	4d 89 d3
add	\$t0, \$t1	4d 01 da

CPU directly executes machine code

Register file $\rho = \left\{ \begin{array}{l} \$v0 \mapsto \dots \\ \$t0 \mapsto \dots \\ \dots \\ \$gp \mapsto \dots \end{array} \right\}$

Read: $\rho(\$r)$

Update: $[\$r := x]\rho$



Operational Semantics

Register file $\rho = \left\{ \begin{array}{l} \$v0 \mapsto \dots \\ \$t0 \mapsto \dots \\ \dots \\ \$gp \mapsto \dots \end{array} \right\}$

li $\$r, v$

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Read: $\rho(\$r)$

Update: $[\$r := x]\rho$

li $\$r, v | \rho \longrightarrow$

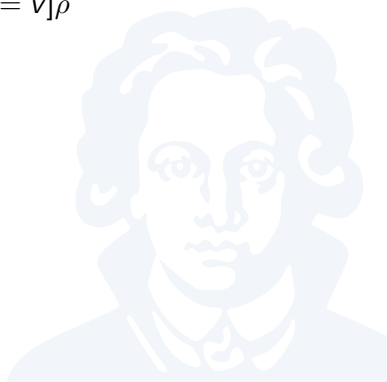


Register file $\rho = \left\{ \begin{array}{l} \$v0 \mapsto \dots \\ \$t0 \mapsto \dots \\ \dots \\ \$gp \mapsto \dots \end{array} \right\}$

Read: $\rho(\$r)$

Update: $[\$r := x]\rho$

li $\$r, v | \rho \longrightarrow \varepsilon | [\$r := v]\rho$



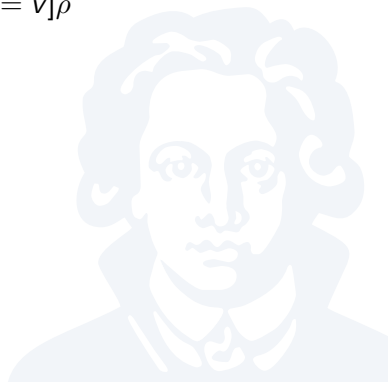
Operational Semantics

Register file $\rho = \left\{ \begin{array}{l} \$v0 \mapsto \dots \\ \$t0 \mapsto \dots \\ \dots \\ \$gp \mapsto \dots \end{array} \right\}$

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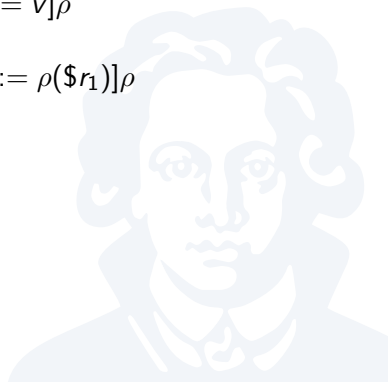
move $\$r_0, \$r_1 | \rho$



Register file $\rho = \left\{ \begin{array}{l} \$v0 \mapsto \dots \\ \$t0 \mapsto \dots \\ \dots \\ \$gp \mapsto \dots \end{array} \right\}$ **Read:** $\rho(\$r)$
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move $\$r_0, \$r_1 | \rho \longrightarrow \varepsilon | [\$r_0 := \rho(\$r_1)]\rho$



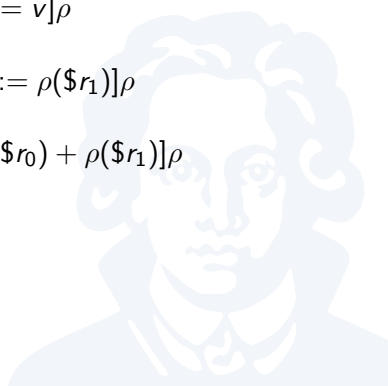
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$$\text{Register file } \rho = \left\{ \begin{array}{l} \$v0 \mapsto \dots \\ \$t0 \mapsto \dots \\ \dots \\ \$gp \mapsto \dots \end{array} \right\} \quad \begin{array}{l} \text{Read: } \rho(\$r) \\ \text{Update: } [\$r := x]\rho \end{array}$$

$$\mathbf{li} \ \$r, v | \rho \longrightarrow \varepsilon | [\$r := v]\rho$$

$$\mathbf{move} \ \$r_0, \$r_1 | \rho \longrightarrow \varepsilon | [\$r_0 := \rho(\$r_1)]\rho$$

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Operational Semantics

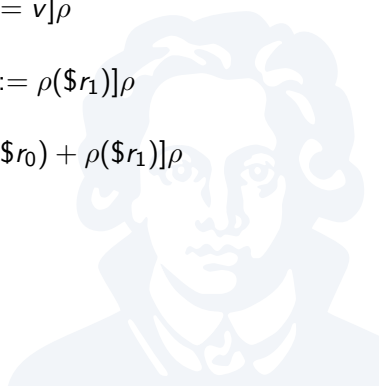
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$$\frac{i_0 | \rho \longrightarrow \varepsilon | \rho'}{i_0; i_1 | \rho \longrightarrow i_1 | \rho'}$$



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Rule for **add** not quite accurate!

Overflow

- ▶ Real CPUs operate only on 64 bits:
`0x8000000000000000 + 0x8000000000000001`



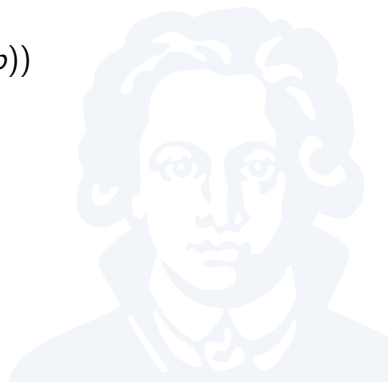
Overflow

- ▶ Real CPUs operate only on 64 bits:
 $0x8000000000000000 + 0x8000000000000001 = 1$
Overflow



Overflow

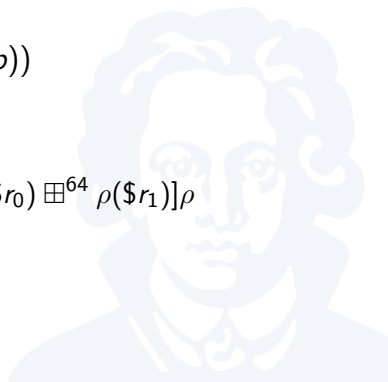
- ▶ Real CPUs operate only on 64 bits:
 $0x8000000000000000 + 0x8000000000000001 = 1$
Overflow
- ▶ $a + b$ knows no bit bound
- ▶ We define:
$$a \boxplus^k b \equiv \text{repr}^k(\text{num}_s^k(a) + \text{num}_s^k(b))$$
- ▶ Analogous for $\boxminus^k, \boxtimes^k, \dots$



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- ▶ Analogous for \boxminus^k , \boxtimes^k , ...

add $\$r_0, \$r_1 | \rho \longrightarrow \varepsilon | [\$r_0 := \rho(\$r_0) \boxplus^{64} \rho(\$r_1)] \rho$



Arithmetic

Additional operations for:

- ▶ Arithmetic: **sub**, **mul**, **div_a2v0**

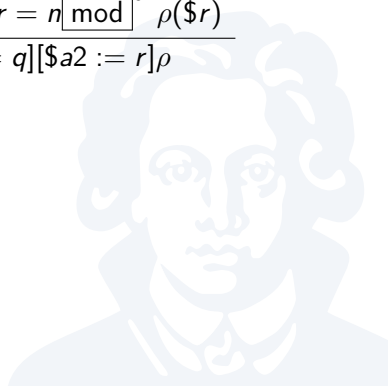


Arithmetic

Additional operations for:

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$$\frac{\rho(\$r) \neq 0 \quad n = \rho(\$a2) : \rho(\$v0) \quad q = n \boxed{/}^{64} \rho(\$r) \quad r = n \boxed{\text{mod}}^{64} \rho(\$r)}{\mathbf{div_a2v0} \quad \$r | \rho \longrightarrow \varepsilon | [\$v0 := q][\$a2 := r] \rho}$$



Arithmetic

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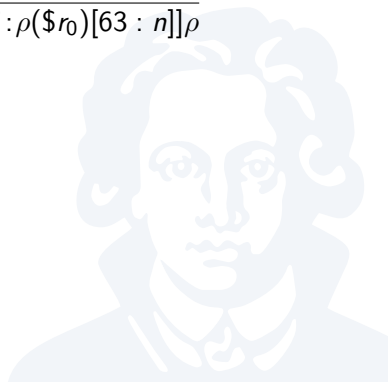
Semantics of realistic CPUs can be complicated!

- ▶ Negation: **not**
- ▶ Bit-Shift: **sll**, **srl**, **sra**
- ▶ Bit combinations: **and**, **or**, **xor**



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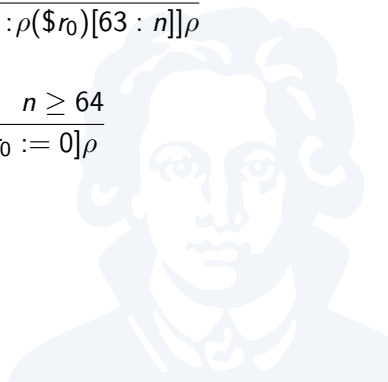
$$\frac{n = \text{num}_u^8(\rho(\$r_1)[7 : 0]) \quad n < 64}{\mathbf{srl} \ \$r_0, \$r_1 | \rho \longrightarrow \varepsilon | [\$r_0 := [0]^n : \rho(\$r_0)[63 : n]] \rho}$$



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Immediate Operations

```
li $t0, 8  
srl $t1, $t0
```

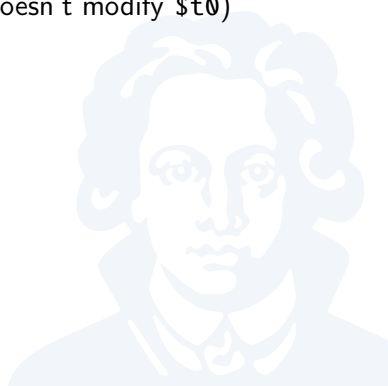


Immediate Operations

Equivalent

```
li $t0, 8  
srl $t1, $t0
```

```
srli $t1, 8  
(but doesn't modify $t0)
```



Immediate Operations

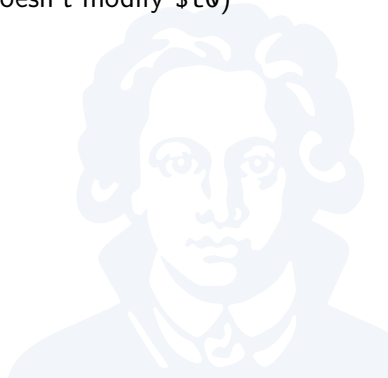
Equivalent

```
li $t0, 8  
srl $t1, $t0
```

```
srli $t1, 8  
(but doesn't modify $t0)
```

Immediate operations:

- ▶ **addi, subi**
- ▶ **slli, srli, srai**
- ▶ **andi, ori, xori**



Summary

- ▶ 2OPM: synthetic assembly language
- ▶ Uses 16 general-purpose registers plus program counter
- ▶ Most operations use two register operands
- ▶ Operations for loading (**li**), copying (**move**)
- ▶ Basic arithmetic with combined division/modulo
- ▶ Bit-wise operations
- ▶ *Immediate* operations with register plus immediate operand available in many cases
- ▶ Describing semantics requires *register file*

Instructions are more fully described in documentation